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ZAGORIN, O'BRIEN & GRAHAM, L.L.P.

Intellectual Property Attorneys

7600B N. CAPITAL OF TEXAS HWY, SUITE 350
AUSTIN, TEXAS 78731

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| To: Examiner Connie C. Yoha | Fax No.: 703-872-9306 |
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| From: Andrew C. Graham Reg. No. 36,531 | Sender's Phone No.: 512-338-6300 |
| | Sender's Fax No.: 512-338-6301 |

REGARDING:

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|------------------------------------|--|-------------------|--|
| Title: | INTEGRATED CIRCUIT MEMORY ARRAY WITH FAST TEST MODE UTILIZING MULTIPLE WORD LINE SELECTION AND METHOD THEREFOR | | |
| Application No.: 09/990,894 | Filed: | November 16, 2001 | |
| Examiner: Connie C. Yoha | Group Art Unit: | 2818 | |
| Atty. Docket No.: 023-0013 | Confirmation No.: | 3451 | |

ATTACHED HERETO:

(1) Response to Non-Final Office Action (9) pages;

CERTIFICATE OF FACSIMILE TRANSMISSION

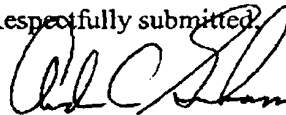
I hereby certify that, on the date shown below, this
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Andrew C. Graham

Date

1-20-04

Respectfully submitted,



Andrew C. Graham, Reg. No. 36,531
Attorney for Applicant(s)
(512) 338-6313 (direct)
(512) 338-6301 (fax)

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PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JAN 20 2004

Applicant(s): Roy E. Scheuerlein

Title: INTEGRATED CIRCUIT MEMORY ARRAY WITH FAST TEST MODE
UTILIZING MULTIPLE WORD LINE SELECTION AND METHOD
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Application No.: 09/990,894

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Confirmation No.: 3451

January 20, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE NON-FINAL TO OFFICE ACTION

This paper is responsive to the Non-Final Office Action dated October 20, 2003, having a shortened statutory period for response set to expire January 20, 2004. In light of the Amendments and/or Remarks herein, further examination is requested.

No fee is believed due with this paper. If, however, a fee is determined to be required by this paper, please charge deposit account 50-0631 for such required fee.